High Gain and High Efficiency K-Band Power HEMT with WSi/Au T-Shaped Gate

T. Kunii, N. Yoshida, S. Miyakuni, T. Shiga, T. Oku, T. Kitano, J. Udomoto,
M. Komaru, A. Inoue, S. Tsuji *, N. Tanino, T. Ishikawa, and Y. Mitsui

Optoelectronic and Microwave Devices Laboratory,
High Frequency & Optical Semiconductor Division *
Mitsubishi Electric Corporation
4-1, Mizuhara, Itami, Hyogo 664, Japan
TEL:+81-727-84-7386 FAX:+81-727-80-2694
email : kuniii@oml.melco.co.jp

ABSTRACT

We have developed WSi/Au T-shaped buried gate pseudomorphic HEMT with the good uniformity of recess current by using a selective etching process and with a high off-state break down voltage of over 19V. A 1.4W output power has been obtained with a power-added efficiency of 55.6% and an associated gain of 9.2dB under high voltage operation of Vd=10V at 18GHz. This is the highest gain and efficiency achieved by a single FET chip with over a watt output power at this frequency.

I. INTRODUCTION

Solid-state power amplifiers (SSPAs) have numerous advantages such as low cost, small size, light weight, and high reliability in comparison with traveling-wave tube amplifiers (TWTAs). SSPAs have been replacing TWTAs at C to Ku-Band frequencies in recent satellite communication systems. Nowadays K-Band SSPAs are increasingly required for the satellite communication systems to secure more information traffic. Many works have been performed in order to improve the RF performance of solid-state power transistors, especially gain and efficiency, at K-Band [1-6]. Recently, according to the progress of the phased-array antenna in satellite communication systems, a number of small sized power amplifiers with high output power, high gain and high efficiency are required for the systems. To meet the system requirements, high power density under high voltage operation with better uniformity in device performance is required for the SSPAs.

We have developed a WSi/Au T-shaped buried gate pseudomorphic HEMT by using selective etching process for uniform recess current, and by using sidewall forming processes for a reliable gate electrode. Off-state break down voltage as high as 19V is obtained, which is advantageous to high power density operation because high drain bias voltage is required for it. The developed devices demonstrate 1.4W output power with a power-added efficiency of 55.6% and an associated gain of 9.2dB at 18GHz. K-Band solid-state power transistors performances

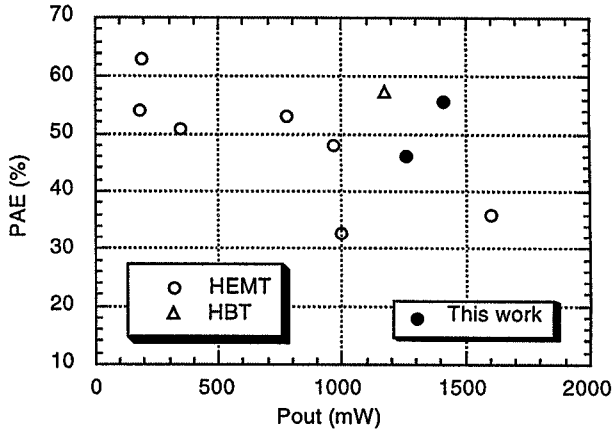
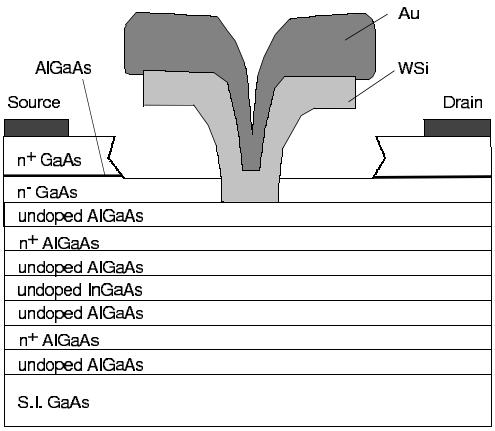
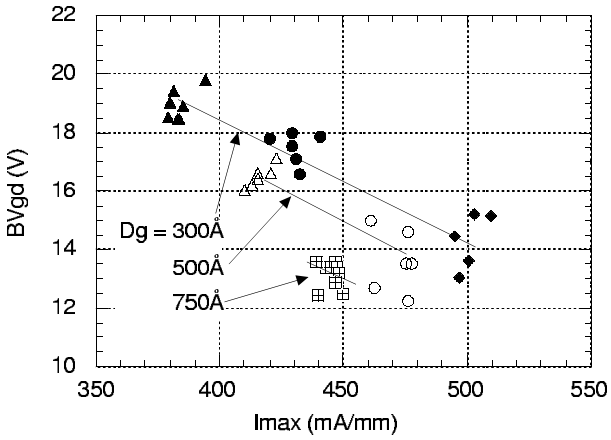
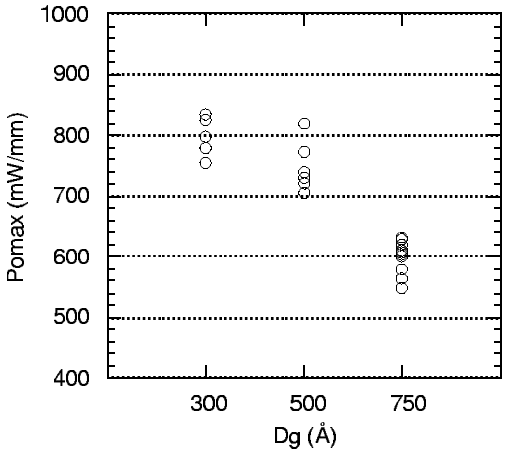


Fig. 1 Power performance of transistors at K-band

0-7803-4603-6/97/$5.00 (c) IEEE







that have been reported so far [1-6] are plotted in Fig.1, including this work. This figure indicates that our work exceeds others in terms of output power, power-added efficiency and associated gain.

II. DEVICE FABRICATION

A schematic cross-section of a developed pseudomorphic HEMT with a WSi/Au T-shaped buried gate is shown in Fig.2. The material structure of this device includes an undoped InGaAs channel layer sandwiched between a couple of highly doped AlGaAs electron supply layers in order to obtain a high current density. On the upper highly doped AlGaAs layer, a highly doped GaAs cap layer, thin AlGaAs etch stop layer, low doped GaAs layer, and undoped AlGaAs Shottky layer are employed. Three key points of the gate electrode fabrication are described as follows. The first point is the realization of the buried gate structure in order to reduce the influence of surface depletion layer. In order to attain a higher production yield in the sub-half micron buried gate process, we employed SiO2 sidewalls and an dry-etching technique [7-8]. The second point is that we employed WSi as a schottky metal for higher reliability [7] and adopted gold on the WSi for reducing gate resistance. The third point is to achieve the uniform current among fingers in a chip as well as that in an entire wafer by developing a double selective recess etching technique. The first wide wet recess etching was selectively stopped on the thin AlGaAs layer by using citric acid-based etchant [9]. The second gate recess was formed by selectively dry-

μm and a gold plated heat sink (PHS) structure was adopted on the backside of the wafer. The device with a total gate width of 2.1mm (1.05mm FET×2) was measured for power characteristics.

At first, we optimized the depth of the buried gate. Figure 3 shows the gate-drain breakdown voltage (Bvgd) determined at a reverse current of 100μA/mm as a function of maximum drain current (Imax). This figure indicates that Bvgd depends on the depth of the buried gate (Dg), which corresponds to the low doped GaAs layer thickness (Dg=300Å, 500Å, 750Å). Imax rises with increase of Dg, because of less influence of the surface depletion layer in

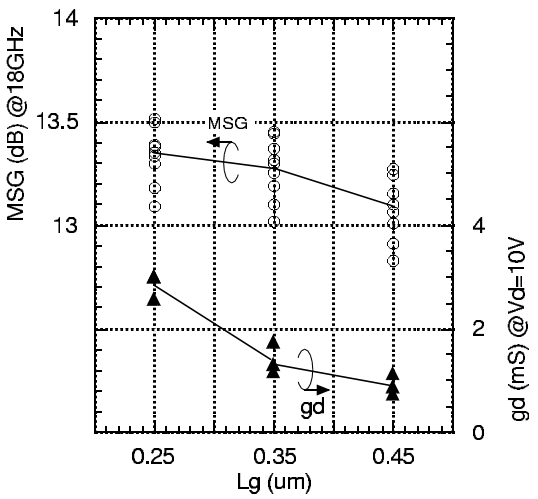
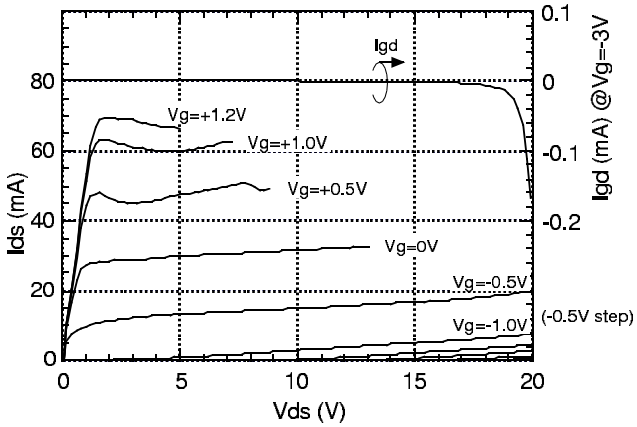
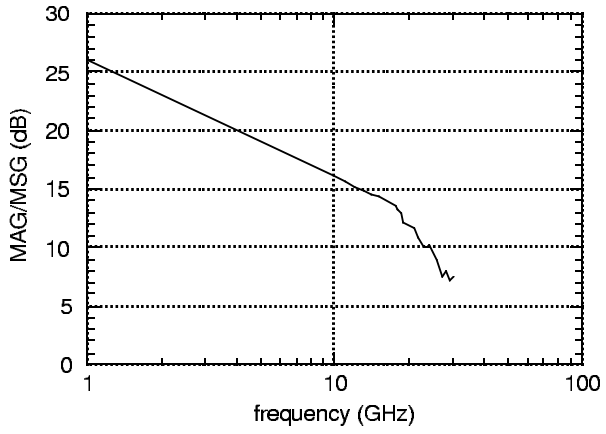
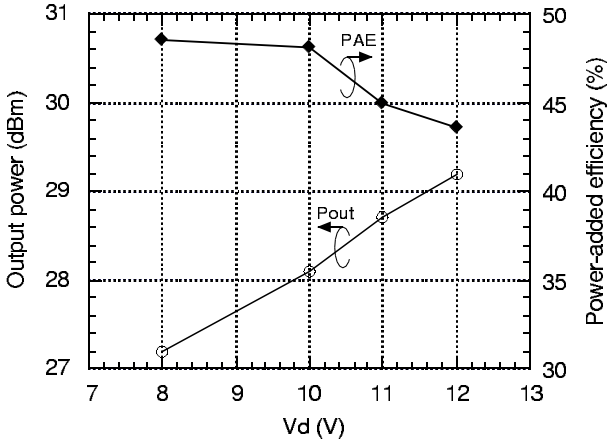


Fig.5 MSG at 18GHz and drain conductance at Vd=10V as a function of gate length







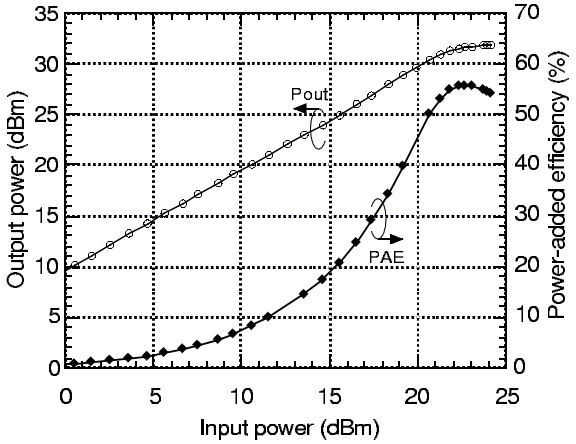
III. CHARACTERISTICS

the vicinity of the gate, while Bvgd increases as Dg decreases. Figure 4 shows the maximum power density (Pomax) calculated by DC parameter as a function of the depth of buried gate (Dg). In order to obtain high power density as well as Bvgd of over 18V, we chose 300Å as the depth of the buried gate.

Figure 5 shows Maximum Stable Gain (MSG) at 18GHz and drain conductance (gd) at Vd=10V of a unit FET (Wg=75μm×14=1050μm) as a function of gate length (Lg). Drain conductance should be low in order to obtain high power-added efficiency, while MSG should be high to obtain a high gain. To achieve both a high power-added efficiency and a high gain, we chose 0.35μm for the gate length.

Figure 6 shows typical Ids-Vds and Igd-Vds characteristics for a 150μm gate (75μm×2) device. A high maximum drain current of 430mA/mm and a high off-state break down voltage (BVds : measured at Ig=1mA/mm, Vg=-3V) of over 19V are obtained, which are advantageous to higher power density operation. The value of gd hardly increases even at Vd=20V in this I-V plot, which is advantageous to high efficiency under high voltage operation. Furthermore, pinch-off voltage (Vp) variation as small as 40mV has been obtained in an entire wafer due to the selective etching process for gate recess.

Figure 7 shows Maximum Available Gain and Maximum Stable Gain (MAG/MSG) of a unit FET as a function of frequency. Because of reduction of gate resistance and



adoption of Wg=75μm×14, the frequency at K=1 is 19GHz, and MSG of a unit gate FET is as high as 13.3dB at 18GHz.

The power characteristics of the device was measured at 18GHz. Figure 8 shows the output power and power-added efficiency of the 1.05mm unit FET for power matched conditions as a function of drain voltage. We obtained a high power-added efficiency of 48% at Vd=10V, owing to the realization of the flatness of gd up to Vd=20V and to the realization of BVds=19V.

Figure 9 shows output power and power-added efficiency for the 2.1mm device for an efficiency matched condition at 18GHz. A 1.4W output power was obtained with a power-added efficiency of 55.6% and an associated gain of 9.2dB at Vd=10V. The power density is 670mW/mm. For a gain matched condition, a 1.26W output power was obtained with a power-added efficiency of 46.0% and an associated gain of 10.7dB at Vd=10V. These are the highest gain and efficiency achieved by a single FET chip with over a watt output power at this frequency.

IV. CONCLUSION

We developed WSi/Au T-shaped buried gate pseudomorphic HEMT with the good uniformity of recess current by using a double selective recess etching technique in fabricating gate recess. The developed device has demonstrated a high off-state break down voltage of over 19V and has delivered a 1.4W output power with a power-added efficiency of 55.6% and an associated gain of 9.2dB

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